WHAT IS CLAIMED IS:

1. A method of planarizing active layers of devices on a semiconductor structure comprising the steps of:

providing a semiconductor structure, said semiconductor structure having a top layer of dielectric material and areas of metallization defined in the top surface of said layer of dielectric material;

depositing TMR devices at selected locations over said areas of metallization, said TMR devices having a known height above said top surface of said top layer of dielectric;

depositing a first dielectric layer over said top surface of said dielectric layer and over said semiconductor devices;

forming a dummy layer of dielectric material over said first dielectric layer to a thickness equal to said known height of said active semiconductor devices;

forming a dummy structure pattern mask over said dummy layer of dielectric material;

etching said dummy layer of dielectric selective to said first dielectric layer so as to leave portions of said dummy layer as dummy structures on said top surface of said top layer of said dielectric, said dummy structure having a height equivalent to said known height;

depositing another layer of dielectric material over said active semiconductor devices and said dummy structures, said another layer of dielectric material having a thickness at least greater than said known height of said semiconductor devices.

2. The method of claim 1 wherein the semiconductor structure is according to an XPC architecture, and the TMR elements are deposited directly on top of the metallization.

3. The method of claim 1 wherein the semiconductor structure is according to an FET architecture, the metallization is covered by a thin insulation layer, the TMR elements are deposited on top of said thin insulation layer and are connected by a local interconnect to an adjacent read wire.

4. The method of claim 1 wherein said TMR structure comprises at least two layers of metallization.

5. The method of claim 1 wherein said first dielectric conformal layer is resistant to the diffusion of copper atoms and ions.

6. The method of claim 3 wherein said step of depositing a first dielectric layer comprises the step of depositing a layer selected from the group consisting of silicon nitride (Si_3N_4), Silicon oxy nitride (SiON), silicon carbide (SiC) and aluminum oxide (Al_2O_3).

7. The method of claim 3 wherein said step of depositing another layer of dielectric material comprises the step of depositing a layer of silicon oxide (SiO_2).

8. The method of claim 3 wherein said step of depositing another layer of dielectric material comprises the step of depositing a layer of a low K dielectric.

9. The method of claim 5 further comprising the steps of:

etching wire trenches in said silicon oxide layer down to said coating of silicon nitride;

further etching vias through said coating of silicon nitride in selective ones of said trenches to said lines of metallization in said top layer of dielectric; and

filling said trenches and vias with a conductive metal.

10. The method of claim 7 wherein said steps of etching trenches and vias comprises forming an etch mask with lithography and reactive ion etching said silicon oxide.

11. The method of claim 1 wherein said step of etching said another layer of dielectric comprises the step of patterning a hardmask with MUV (mid-ultraviolet) lithography and etching said another layer of dielectric with an oxide etch selective to silicon nitride.

12. The method of claim 1 wherein active semiconductor devices include Tunnel Junction devices.

13. The method of claim 8 wherein said conductive metal is copper.

14. The method of claim 1 wherein said step of etching dummy structures comprises the steps of depositing said layer of dielectric to a thickness equivalent to said known height, and etching to remove all of said dummy layer except those portions protected by the photoresist mask.

15. The method of claim 1 wherein said step of depositing active semiconductor elements is according to the pattern factor rules for fill structures and during planarization for MRAM structures and said step of forming dummy structures follows less stringent rules and uses MUV (Mid-UltraViolet) lithography.

16. The method of claim 7 further comprising the step of depositing a coating of TaN (tantalum nitride) over trenches and vias.

17. The method of claim 4 wherein said step of etching dummy structures comprises the step of depositing said dummy layer to a thickness substantially equal to said known height, etching

said dummy layer with a process selective to said first conformal dielectric layer and stripping said photoresist mask to leave said dummy structures.